

11017 U.S. PTO
10/083163



U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10083163	FILING DATE 02/27/2002	CLASS 357 438	SUBCLASS 377	GA 2826 2812	EXAMINER Dickey
----------------------	---------------------------	---------------------	-----------------	--------------------	--------------------

**APPLICANTS: Hokazono Akira; *TH*

**CONTINUING DATA VERIFIED:

None TH

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-392569 12/25/2001 *TH*

PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no Verified and Acknowledged Examiners's initials <i>TH</i>		ATTORNEY DOCKET NO 220110US2S
TITLE : Semiconductor device having active regions connected together by interconnect layer and method of manufacture thereof		

U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)

BEST AVAILABLE COPY

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
			Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner PREPARED FOR ISSUE Application Examiner	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)